PC133 SDRAM Unbuffered DIMM Specification

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Prepared by:
VIA Technologies
IBM Microelectronics
Micron Semiconductor Products
NEC Electronics
Samsung Semiconductor

Related Documents

Intel® PC100 SDRAM Unbuffered DIMM Specification
Intel® PC100 SDRAM Reference Designs
JEDEC Publication 95 MO161 - Microelectronics Outlines
JEDEC JCB-99-32 - 133 MHz SDRAM Timing Specification
JEDEC JCB-99-31 - 133 MHz SDRAM Capacitance Specification
JEDEC JESD 21-C Section 4.1 - Serial Presence Detect Standard
JEDEC JESD 21-C Section 4.5.4 (JC42.5-96-146A) - 168-pin Unbuffered SDRAM DIMM Standard

JEDEC documents are available at http://www.jedec.org
Intel® PC100 documents are available at http://developer.intel.com/design/chipsets/memory/sdram.htm

Revision History

Document Release	Release Date	Revised Page(s)	Description of Change	Initials
0.1	5/7/99	all	Initial Release for Review	DH
0.2	5/17/99	2	Removed VIA copyright notice to comply with JEDEC requirements	DH
0.3	5/18/99	4, 6, 8-26	Fixed typos in pin descriptions, module configuration table, DIMM labeling Fixed JEDEC document numbers, mechanical dimensions, & block diagrams Modified AC timing TRP, TRCD, TACN, TOHN and DC Ambient Temperature Modified SPD intro, table title, & example bytes 4, 23, and 24	DH
0.4	6/7/99	19-21, 24	AC Timing Table - Format changed to combine CL2 and CL3 columns SPD Example - Changed bytes 23-24 to 10 & 6 ns to match 2-2-2 timing Modified labeling spec to remove revision # (use latest Intel 1.0 layouts)	DH

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1. Introduction and Overview

This specification defines the electrical and mechanical requirements for 168-pin, 3.3 Volt, 133MHz, 64 / 72-bit wide, Unbuffered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in PC systems.

Reference design examples are included which provide an initial basis for Unbuffered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for 133MHz support. All Unbuffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the "168-pin 8-Byte Unbuffered SDRAM DIMM" standard defined by JEDEC. (Refer to JEDEC document number JESD 21-C Section 4.5.4)

DIMM Attributes

DIMM Organization	x 72 ECC, x 64 Non-ECC
DIMM Dimensions (nominal)	5.25" x 1.5"/1.7" x .163"
Pin Count	168
SDRAMs Supported	64Mb, 128Mb, and 256Mb with x8 and x16 devices
Capacity	32 MB, 64MB, 128MB, 256MB, 512MB
Serial Presence Detect (SPD)	Consistent with JEDEC Rev. 2.0
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

2. Pinouts

Pin Summary

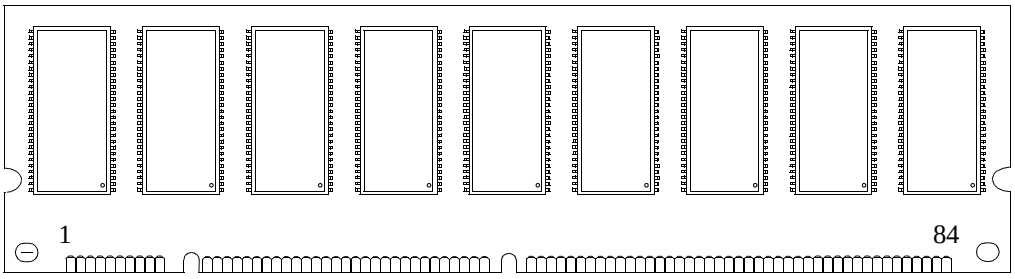
Symbol	Type	Symbol	Type
CK (0-3)	Clock Inputs	DQ (0-63)	Data Input / Output
CKE (0-1)	Clock Enables	CB (0-7)	ECC Data Input / Output
RAS#	Row Address Strobe	DQMB (0-7)	Data Mask
CAS#	Column Address Strobe	V_{CC}	Power (3.3V)
WE#	Write Enable	V_{SS}	Ground
S (0-3)#	Chip Selects	SCL	Serial Presence Detect Clock Input
A (0-9,11-13)	Address Inputs	SDA	Serial Presence Detect Data Input / Output
A10 / AP	Address Input / Autoprecharge	SA (0-2)	Serial Presence Detect Address Inputs
BA (0-1)	SDRAM Bank Address	WP	Write Protect for SPD on DIMM
NC	No Connect		

Pin Functional Descriptions

Symbol	Type	Polarity	Function
CK0-3	Input	Positive Edge	The system clock inputs. All SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0-1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
S0# - S3#	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0# and S2#; Bank 1 is selected by S1# and S3#.
RAS#, CAS#, WE#	Input	Active Low	When sampled at the positive rising edge of the clock, RAS#, CAS#, and WE# define the operation to be executed by the SDRAM.
BA0, 1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-13 A10 / AP	Input	—	During a Bank Activate command cycle, A0-A13 (A0-A12 for 64Mb based modules) defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 define the column address (CA0-CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke an autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0-63	Input Output	—	Data Input/Output pins.
CB0-7	Input Output	—	Check Bit Input/Output pins.
DQMB0-7	Input	Active High	The Data Input / Output masks, associated with one data byte each, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB has a latency of two clock cycles, and controls the output buffers like an output enable. In Write mode, DQMB has a zero clock latency. In this case, DQMB operates as a byte mask (low allows input data to be written and high blocks the write operation).
V_{DD}, V_{SS}	Supply		Power and ground for the module.
SA0 - 2	Input	—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the SPD EEPROM.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus to V_{DD} to act as a pull up.
WP	Input	Active High	This signal is pulled low on the DIMM to enable data to be written into the last 128 bytes of the SPD EEPROM.

Pin List

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	S2#	129	S3#	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	WE#	111	CAS#	48	NC	132	A13	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	S0#	114	S1#	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	RAS#	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10 / AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	BA1	123	A11	60	DQ20	144	DQ52	81	WP	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	A12	63	CKE1	147	NC	84	V_{DD}	168	V_{DD}



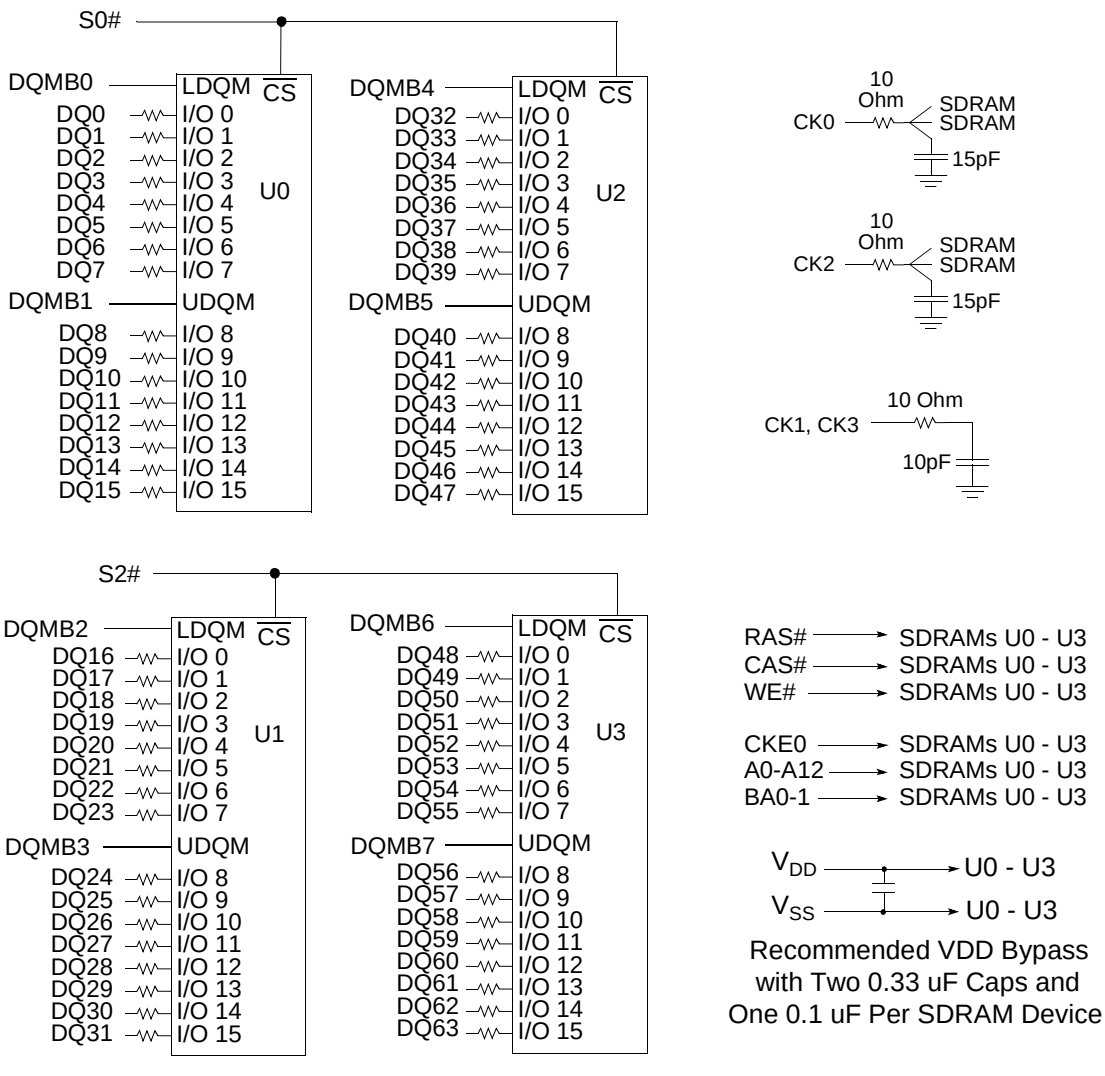
Contacts 1-84 are located on the front side of the DIMM (the component side for single sided DIMMs)
Contacts 85 - 168 are located on the back side of the DIMM (contact 85 is opposite contact 1)

3. Block Diagrams

SDRAM Module Configurations (Reference Designs)

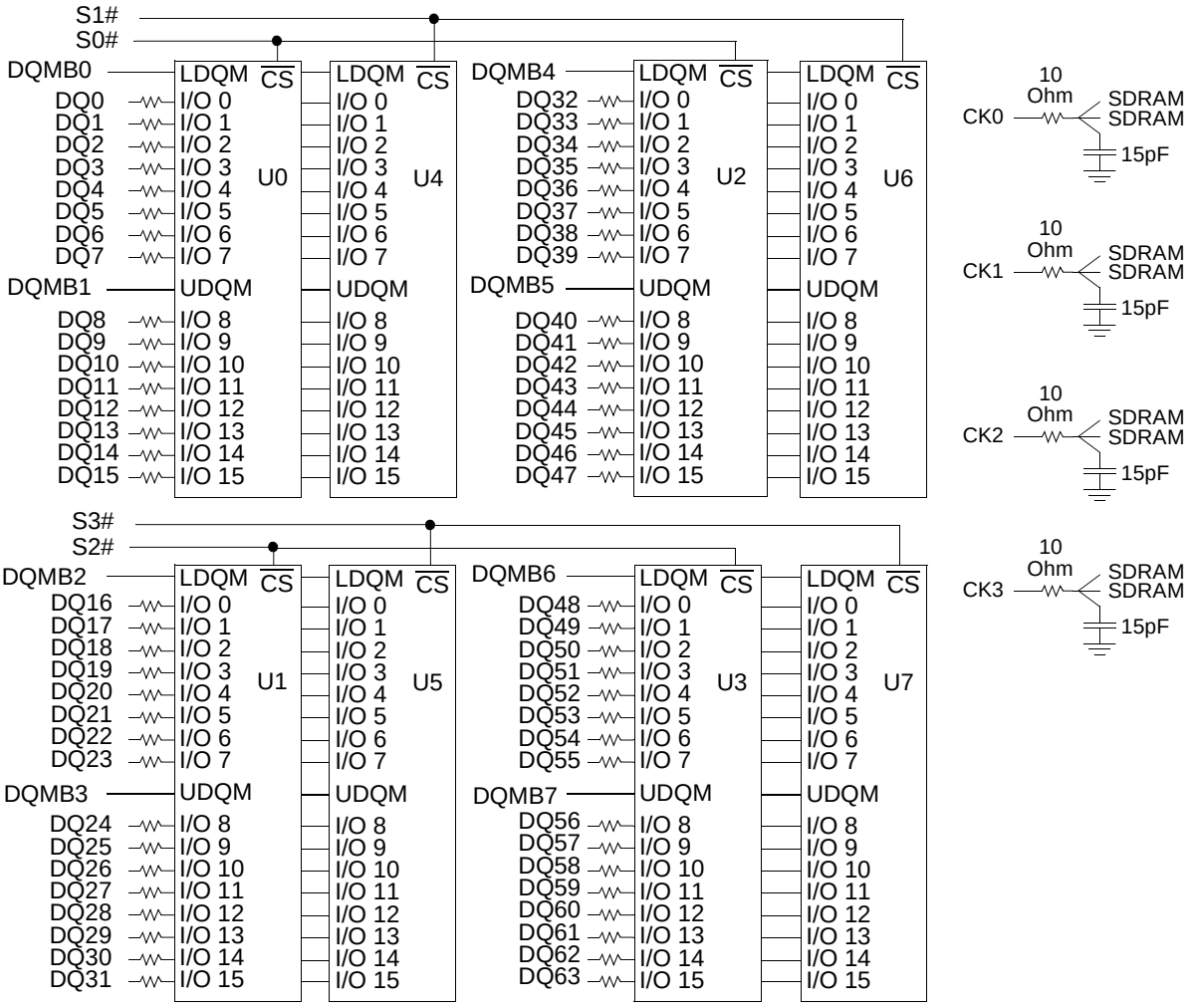
DIMM Configuration	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col/banks
64b SB x16	32MB	4Mx64	64Mbit	4Mx16	4	1	4	12/8/2
64b SB x16	64MB	8Mx64	128Mbit	8Mx16	4	1	4	12/9/2
64b SB x16	128MB	16Mx64	256Mbit	16Mx16	4	1	4	13/9/2
64b DB x16	64MB	8Mx64	64Mbit	4Mx16	8	2	4	12/8/2
64b DB x16	128MB	16Mx64	128Mbit	8Mx16	8	2	4	12/9/2
64b DB x16	256MB	32Mx64	256Mbit	16Mx16	8	2	4	13/9/2
64b SB x8	64MB	8Mx64	64Mbit	8Mx8	8	1	4	12/9/2
64b SB x8	128MB	16Mx64	128Mbit	16Mx8	8	1	4	12/10/2
64b SB x8	256MB	32Mx64	256Mbit	32Mx8	8	1	4	13/10/2
64b DB x8	128MB	16Mx64	64Mbit	8Mx8	16	2	4	12/9/2
64b DB x8	256MB	32Mx64	128Mbit	16Mx8	16	2	4	12/10/2
64b DB x8	512MB	64Mx64	256Mbit	32Mx8	16	2	4	13/10/2
72b SB x16	32MB	4Mx72	64Mbit	4Mx16	5	1	4	12/8/2
72b SB x16	64MB	8Mx72	128Mbit	8Mx16	5	1	4	12/9/2
72b SB x16	128MB	16Mx72	256Mbit	16Mx16	5	1	4	13/9/2
72b DB x16	64MB	8Mx72	64Mbit	4Mx16	10	2	4	12/8/2
72b DB x16	128MB	16Mx72	128Mbit	8Mx16	10	2	4	12/9/2
72b DB x16	256MB	32Mx72	256Mbit	16Mx16	10	2	4	13/9/2
72b SB x8	64MB	8Mx72	64Mbit	8Mx8	9	1	4	12/9/2
72b SB x8	128MB	16Mx72	128Mbit	16Mx8	9	1	4	12/10/2
72b SB x8	256MB	32Mx72	256Mbit	32Mx8	9	1	4	13/10/2
72b DB x8	128MB	16Mx72	64Mbit	8Mx8	18	2	4	12/9/2
72b DB x8	256MB	32Mx72	128Mbit	16Mx8	18	2	4	12/10/2
72b DB x8	512MB	64Mx72	256Mbit	32Mx8	18	2	4	13/10/2

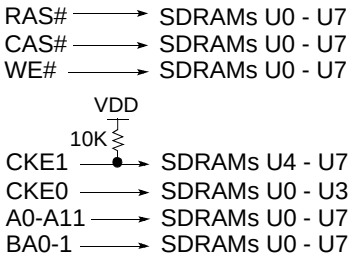
Block Diagram: 64-Bit Single Bank Using x16 Devices



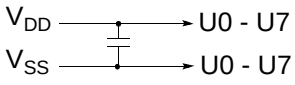
Component U0-3	Module Density
4Mb x 16 SDRAM	32MB
8Mb x 16 SDRAM	64MB
16Mb x 16 SDRAM	128MB

Block Diagram: 64-Bit Dual Bank Using x16 Devices



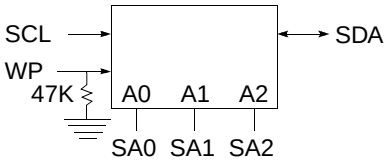


Unless otherwise noted, resistor values are 10 Ohms.



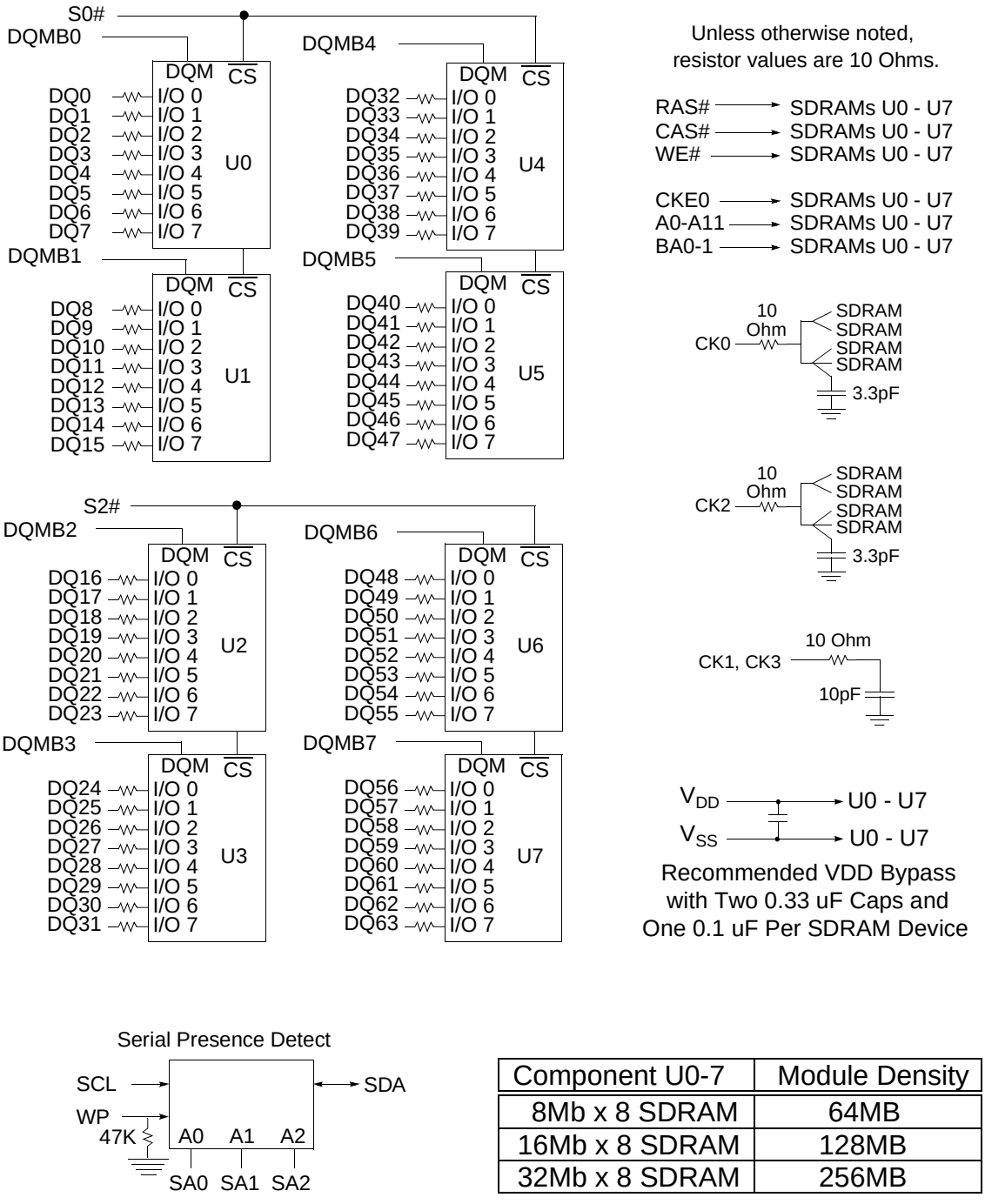
Recommended VDD Bypass with Two 0.33 uF Caps and One 0.1 uF Per SDRAM Device

Serial Presence Detect



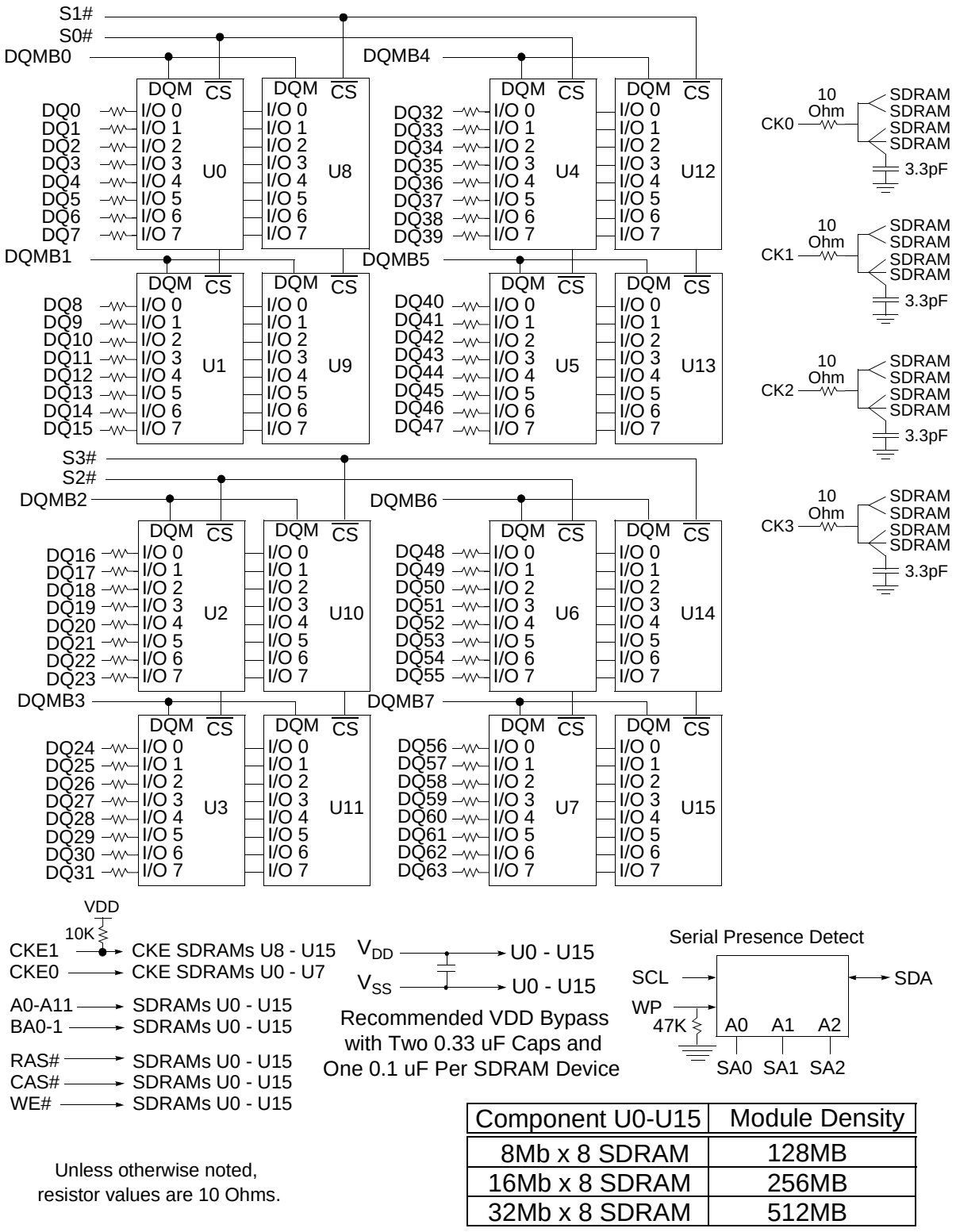
Component U0-7	Module Density
4Mb x 16 SDRAM	64MB
8Mb x 16 SDRAM	128MB
16Mb x 16 SDRAM	256MB

Block Diagram: 64-Bit Single Bank Using x8 Devices



Component U0-7	Module Density
8Mb x 8 SDRAM	64MB
16Mb x 8 SDRAM	128MB
32Mb x 8 SDRAM	256MB

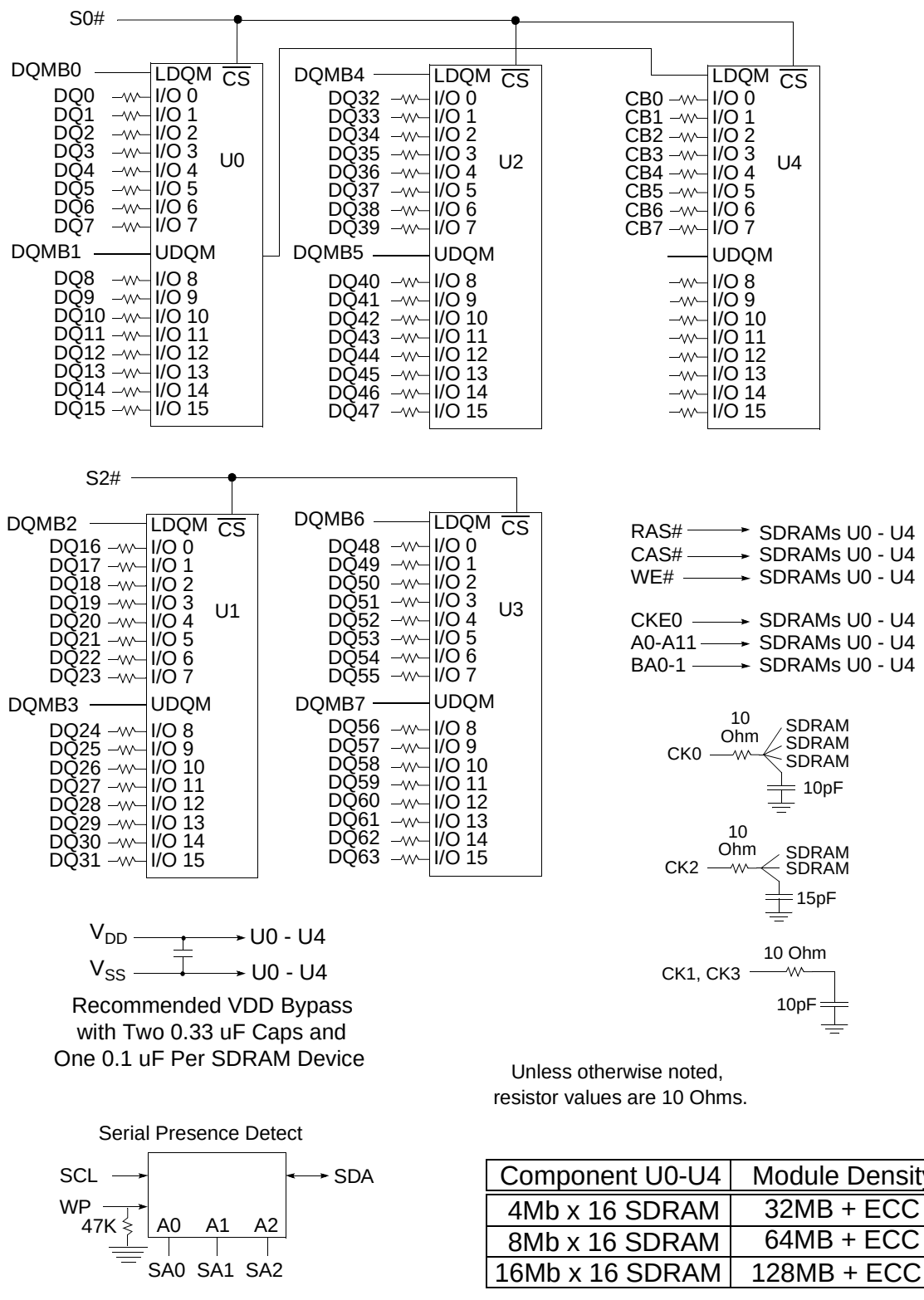
Block Diagram: 64-Bit Dual Bank Using x8 Devices



Unless otherwise noted,
resistor values are 10 Ohms.

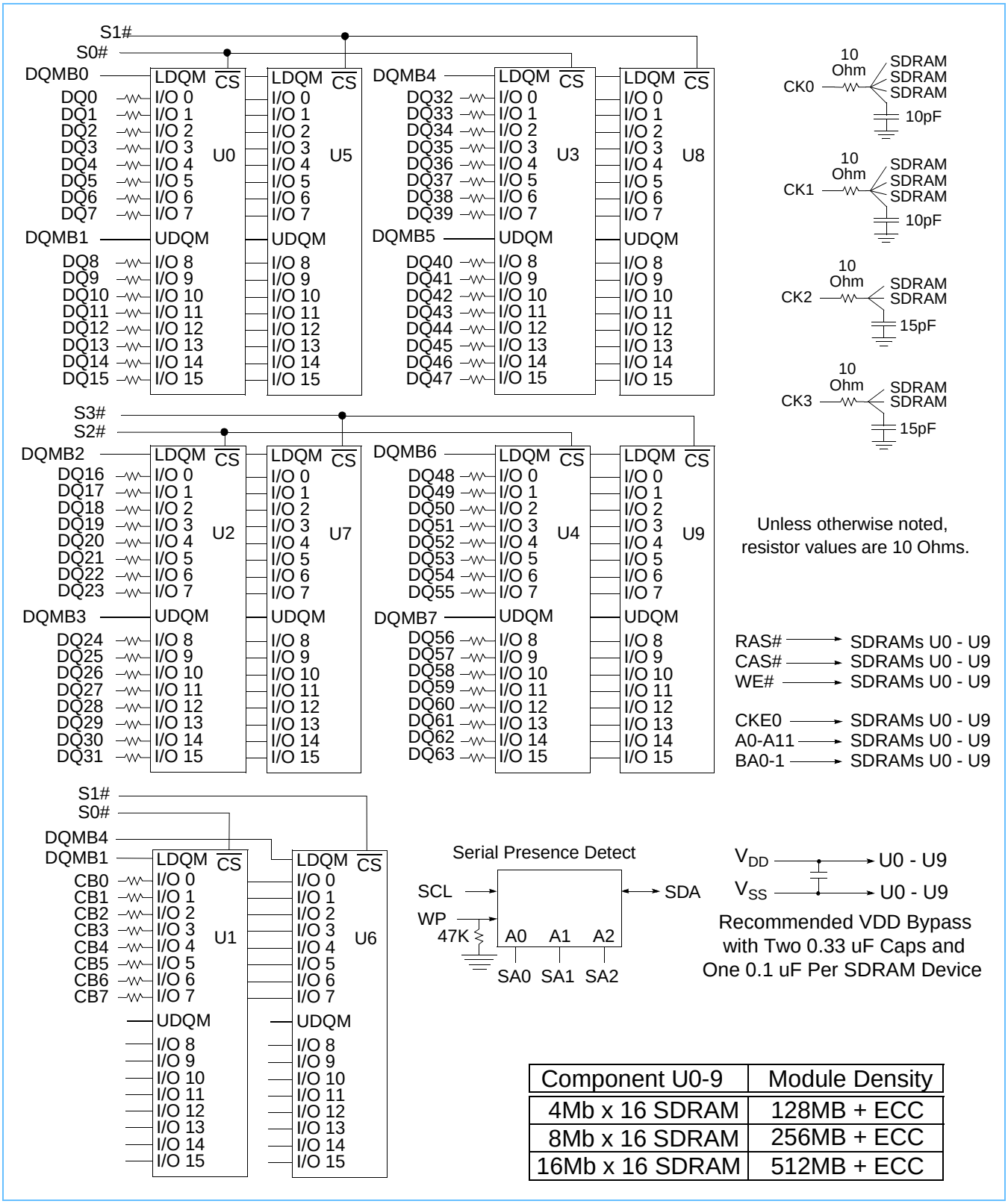
Component U0-U15	Module Density
8Mb x 8 SDRAM	128MB
16Mb x 8 SDRAM	256MB
32Mb x 8 SDRAM	512MB

Block Diagram: 72-Bit Single Bank Using x16 Devices



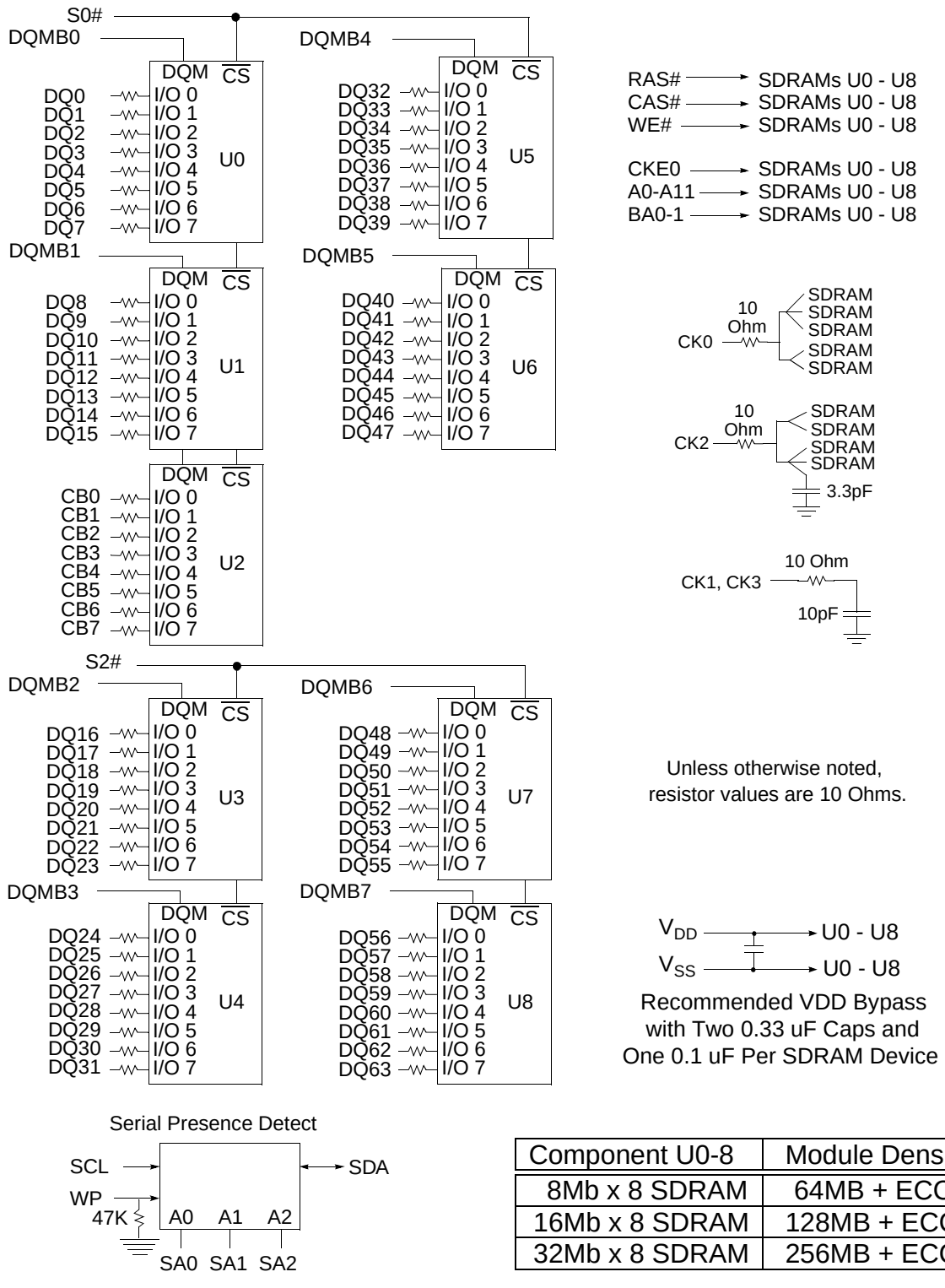
Component U0-U4	Module Density
4Mb x 16 SDRAM	32MB + ECC
8Mb x 16 SDRAM	64MB + ECC
16Mb x 16 SDRAM	128MB + ECC

Block Diagram: 72-Bit Dual Bank Using x16 Devices



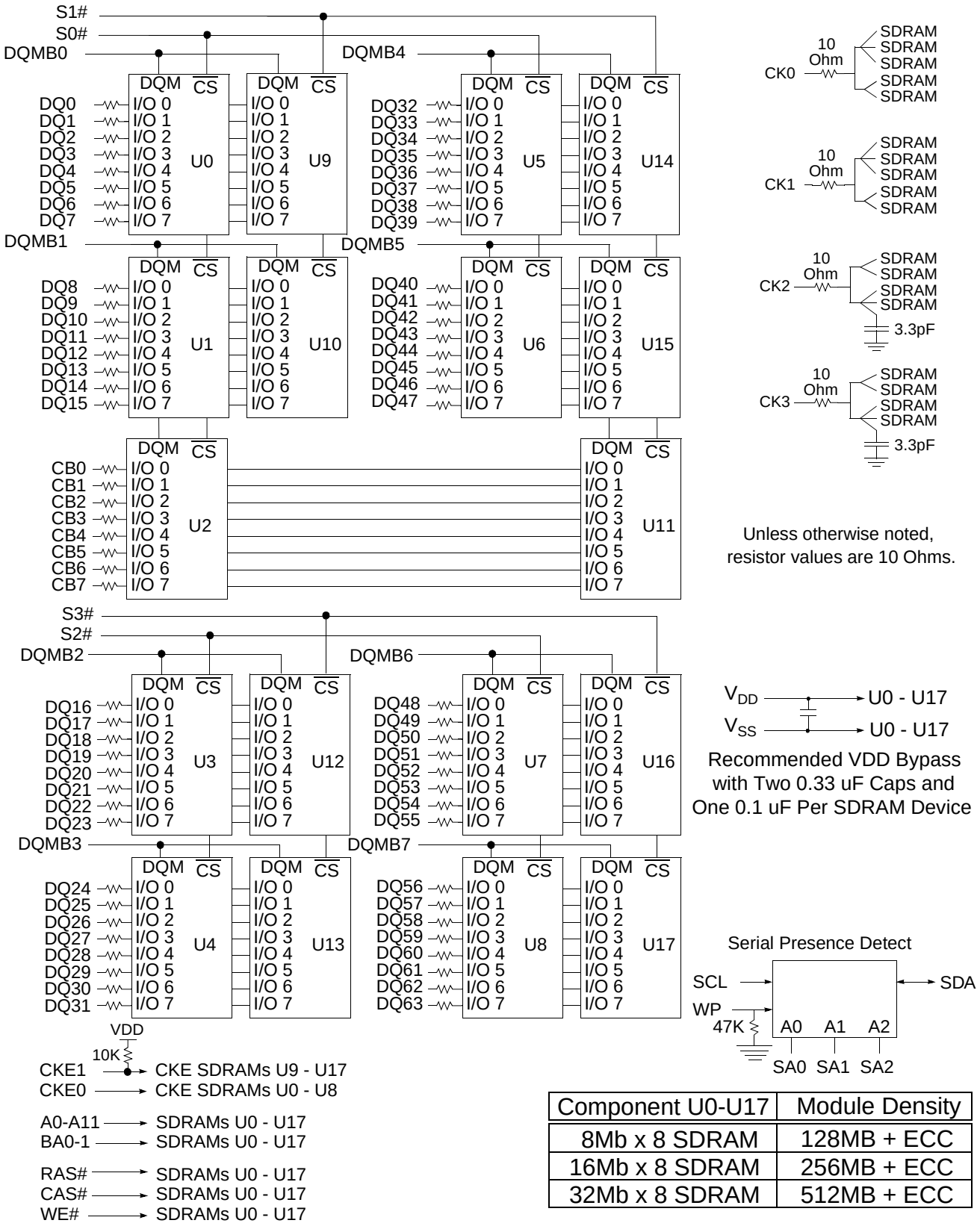
Component U0-9	Module Density
4Mb x 16 SDRAM	128MB + ECC
8Mb x 16 SDRAM	256MB + ECC
16Mb x 16 SDRAM	512MB + ECC

Block Diagram: 72-Bit Single Bank Using x8 Devices



Component U0-8	Module Density
8Mb x 8 SDRAM	64MB + ECC
16Mb x 8 SDRAM	128MB + ECC
32Mb x 8 SDRAM	256MB + ECC

Block Diagram: 72-Bit Dual Bank Using x8 Devices



Component U0-U17	Module Density
8Mb x 8 SDRAM	128MB + ECC
16Mb x 8 SDRAM	256MB + ECC
32Mb x 8 SDRAM	512MB + ECC

4. Electrical and Environmental Specifications

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability .
2. Up to 9850 ft.

PC133 SDRAM Unbuffered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.6	V	
V_{DDQ}	I/O Supply Voltage	3. 0	3.6	V	
Ii_l	Input Leakage Current ($0 < V_{IN} < V_{DDQ}$)	-10	+10	µA	1, 2
I_{CCLP}	I_{cc} Low Power (CKE low, all banks closed)	-	2	ma	
V_{OH}	Output High Voltage (I_{OH} = -4mA)	2.4	-	V	
V_{OL}	Output Low Voltage (I_{OL} = 4mA)	-	0.4	V	
C_{IN}	Input Pin Capacitance (@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{CC}=3.3V)	2.5	3.8	pF	3
$C_{I/O}$	I/O Pin Capacitance(@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{CC}=3.3V)	4.0	6.5	pF	4
C_{CLK}	Pin Capacitance (@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{CC}=3.3v)	2.5	3.5	pF	5
L_{PIN}	Pin Inductance		10	nH	
T_A	Ambient Temperature (No Airflow)	0	65	°C	

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. No Activate or Precharge currents should be included in the Iccac value.
3. Target 3.15pF
4. Target 4.8pF
5. Target 3.0pF

AC Timing Parameters (T_A = 0-65°C; V_{CC} = 3.0V - 3.6V, CL2 or CL3) (Part 1 of 2)

Symbol	Parameter		Min	Max	Units	Notes
T_{CLK}	Clock Period		7.5		ns	
T_{CH}	Clock High Time (Rated @1.5V)		2.5		ns	
T_{CL}	Clock Low Time		2.5		ns	
T_{SI}	Input Setup Times	Address/Command & CKE	1.5		ns	
		Data	1.5		ns	
T_{HI}	Input Hold Times	Address/Command & CKE	0.8		ns	
		Data	0.8		ns	
T_{AC}	Output Valid From Clock	$\overline{CAS}$ Latency = 3 LVTTL levels, Rated @50pF *all outputs switching*		5.4 (T_{ACN} = 4.6)		1
T_{OH}	Output Hold From Clock - 50 pF Load		2.7		ns	
T_{OHN}	Output Hold From Clock - No Load		1.8		ns	
T_{OHZ}	Output Valid to Z		2.7	7	ns	
T_{CCD}	CAS to CAS Delay		1		T_{CLK}	
T_{CBD}	CAS Bank Delay		1		T_{CLK}	
T_{CKE}	CKE to Clock Disable		1		T_{CLK}	
T_{RP}	RAS Precharge Time		15 or 20		ns	
T_{RAS}	RAS Active Time		45		ns	
T_{RCD}	Activate to Command Delay (RAS to CAS Delay)		15 or 20		ns	
T_{RRD}	RAS to RAS Bank Activate Delay		15		ns	
T_{RC}	RAS Cycle Time		67.5		ns	
T_{DQD}	DQM to Input Data Delay		0		T_{CLK}	
T_{DWD}	Write Cmd. to Input Data Delay		0		T_{CLK}	
T_{MRD}	Mode Register set to Active delay		3		T_{CLK}	
T_{ROH}	Precharge to O/P in High Z			CL	T_{CLK}	2
T_{DQZ}	DQM to Data in High Z for read		2		T_{CLK}	

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. T_{ACN} = access time with 0pF load.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit technology, 8192 refresh cycles.

AC Timing Parameters (T_A = 0-65°C; V_{CC} = 3.0V - 3.6V, CL2 or CL3) (Part 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
T_{DQM}	DQM to Data mask for write	0		T_{CLK}	3
T_{DPL}	Data-in to PRE Command Period	15		ns	
T_{DAL}	Data-in to ACT (PRE) Command period (Auto precharge)	5		T_{CLK}	
T_{SB}	Power Down Mode Entry		1	T_{CLK}	
T_{SRX}	Self Refresh Exit Time	10		ns	4
T_{PDE}	Power Down Exit Set up Time	1		T_{CLK}	5
T_{CLKSTP}	Clock Stop During Self Refresh or Power Down	200		T_{CLK}	6
T_{REF}	Refresh Period		64	ms	7
T_{RFC}	Row Refresh Cycle Time	75.0		ns	

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. T_{ACN} = access time with 0pF load.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit technology, 8192 refresh cycles.

5. Serial Presence Detect

The Serial Presence Detect function MUST be implemented on PC133 SDRAM Unbuffered DIMMs. The component used and the data contents must adhere to the most recent versions of the JEDEC SDRAM Serial Presence Detect Specifications. Please refer to these documents for all technical specifications and requirements of the serial presence detect devices.

The table below provides example SPD data for one particular PC133 DIMM configuration. This table may be used as a guide to create the actual SPD contents for other configurations.

Serial Presence Detect Example

Example: 16Mx64 Unbuffered DIMM, PC133 3-3-3, PC100 2-2-2, Dual-Bank Using 8Mx8 (64Mbit) Devices

Byte #	Description	Symbol	SPD Value	SPD Entry	Notes
0	Number of Serial PD Bytes Written during Production		128	80h	
1	Total Number of Bytes in Serial PD device		256	08h	
2	Fundamental Memory Type		SDRAM	04h	
3	Number of Row Addresses on Assembly		12	0Ch	
4	Number of Column Addresses on Assembly		9	09h	
5	Number of DIMM Banks		2	02h	
7 - 6	Data Width of Assembly		x64	4000h	
8	Assembly Voltage Interface Levels		LVTTL	01h	
9	SDRAM Device Cycle Time (CL = 3)	T_{CK}	7.5ns	75h	1
10	SDRAM Device Access Time from Clock at CL= 3	T_{AC}	5.4ns	54h	
11	Assembly Error Detection/Correction Scheme		Non-ECC	00h	
12	Assembly Refresh Rate/Type		SR/1X(15.625µs)	80h	
13	SDRAM Device Width		x8	08h	
14	Error Checking SDRAM Device Width		-	00h	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	T_{CCD}	1 Clock	01h	
16	SDRAM Device Attributes: Burst Lengths Supported		1, 2, 4, 8, Full Page	8Fh	
17	SDRAM Device Attributes: Number of Device Banks		4	04h	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported		2, 3	06h	
19	SDRAM Device Attributes: $\overline{CS}$ Latency		0	01h	
20	SDRAM Device Attributes: $\overline{WE}$ Latency		0	01h	
21	SDRAM Module Attributes		Unbuffered	00h	
22	SDRAM Device Attributes: General		Write-1 / Read Burst, Precharge All, Auto-Precharge	0Eh	
23	Minimum Clock Cycle at CL = 2	T_{CK}	10 ns	A0h	1
24	Maximum Data Access Time from Clock at CL = 2	T_{AC}	6.0 ns	60h	

1. Minimum application clock cycle time is 7.5ns (133MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ‘ 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ‘ 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. These values apply to PC100 applications only, per Intel® PC66/100 SPD standards.

Serial Presence Detect Example

Example: 16Mx64 Unbuffered DIMM, PC133 3-3-3, PC100 2-2-2, Dual-Bank Using 8Mx8 (64Mbit) Devices

Byte #	Description	Symbol	SPD Value	SPD Entry	Notes
25	Minimum Clock Cycle Time at CL = 1	T_{CK}	n/a	00h	
26	Maximum Data Access Time from Clock at CL = 1	T_{AC}	n/a	00h	
27	Minimum Row Precharge Time	T_{RP}	20ns	14h	
28	Minimum Row Active to Row Active Delay	T_{RRD}	15ns	0Fh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	T_{RCD}	20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	T_{RAS}	45.0ns	2Dh	
31	Module Bank Density		64MB	10h	
32	Address and Command Setup Time Before Clock	T_{AS},T_{CMS}	1.5ns	15h	
33	Address and Command Hold Time After Clock	T_{AH},T_{CMH}	0.8ns	08h	
34	Data Input Setup Time Before Clock	T_{DS}	1.5ns	15h	
35	Data Input Hold Time After Clock	T_{DH}	0.8ns	08h	
36-61	Reserved		Undefined	00h	
62	SPD Revision		JEDEC 2	02h	
63	Checksum for bytes 0 - 62			cc	2
64-71	Manufacturers' JEDEC ID Code				
72	Assembly Manufacturing Location				
73-90	Assembly Part Number				
91-92	Assembly Revision Code				
93-94	Assembly Manufacturing Date				3, 4
95-98	Assembly Serial Number				5
99-125	Reserved				
126	Reserved			64h	6
127	Reserved			85h	6
128-255	Open for Customer Use		Undefined	00h	

1. Minimum application clock cycle time is 7.5ns (133MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. These values apply to PC100 applications only, per Intel® PC66/100 SPD standards.

6. Signal Routing and PCB Layout

DIMM signal routing and PCB layouts for PC133 are the same as PC100. Refer to the most recent revision of the Intel® "PC100 SDRAM Unbuffered DIMM Specification" document, available at http://developer.intel.com/design/chipsets/memory/sdram.htm.

7. Labeling

The following label should be applied to all PC133-compatible DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silkscreened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

Format:

PC133m-abc-dde-f

Where:

m: Module Type
- U = Unbuffered DIMM (no registers on DIMM)

a: SDRAM CAS Latency

b: SDRAM minimum t_{RCD} specification (in clocks)

c: SDRAM minimum t_{RP} specification (in clocks)

dd: SDRAM t_{AC} specification (into 50pF load), with no decimal point
- 54= 5.4ns t_{AC}

e: JEDEC SPD Revision used on this DIMM
- 2 = JEDEC SPD Revision 2.0

f: Gerber file used for this design (if applicable)
- A: Intel® PC100 x8 Based, revision 1.0
- B: Intel® PC100 x8 Based Low Cost (LC), revision 1.0
- C: Intel® PC100 x16 Based, revision 1.0
- Z: None of the 'Reference' designs were used on this assembly

Example:

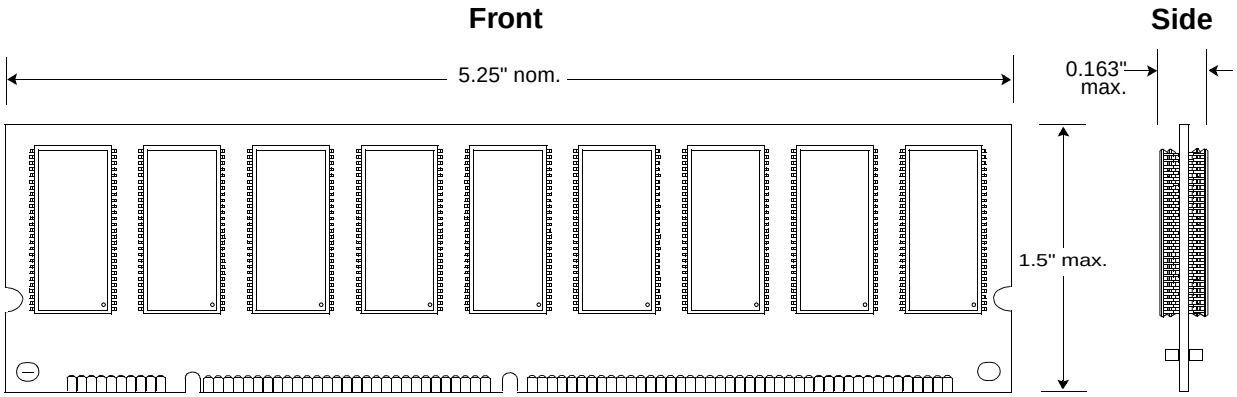
PC133U-333-542-B
is a PC133 Unbuffered DIMM
with CL = 3, t_{RCD} = 3, t_{RP} = 3
and a t_{AC} = 5.4ns, using JEDEC SPD Revision 2
and produced based on the latest Intel x8 based LC Gerber

8. Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 168 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards and Docs.’
3. Scroll down and double click on ‘Publication 95.’
4. Under ‘Outlines/Registrations,’ click on ‘Microelectronics Outlines.’
5. Scroll down and select ‘MO-161’ to download the PDF for this product family.

Simplified Mechanical Drawing with Keying Positions



Note:
The keying defines the DIMM as a 3.3V Unbuffered DIMM with Serial PDs.

- The center key position defines the voltage for the DIMM. For PC133, this key is in the center of the opening, defining this as a 3.3V DIMM.
- The left key position defines the architecture of the DIMM. For PC133, this key is in the right portion of the opening, defining the DIMM as a ’second generation’ 168 pin DIMM with serial PDs.

Appendix A - Supporting Hardware

Clock Reference Board

To facilitate the measurement of clock arrival time to the SDRAM for both PC100 / PC133 Registered and PC100 Unbuffered SDRAM DIMMs, a 'Clock Reference Board' has been designed and released. The board is available from CST (see http://www.simmtester.com).

The clock driver on the reference board has not been optimized for use with Unbuffered DIMMs operating at 133 MHz, and there is no supplier modifiable circuitry in the clock path to adjust clock timings. Therefore, the clock reference board is NOT recommended for use on PC133 Unbuffered DIMMs.

Appendix B - Validation Program

A PC133 validation program has been set up for verification of proper operation of PC133 Memory Devices and DIMMs. For more information refer to the PC133 portion of the VIA Technologies web site at http://www.via.com.tw/news/pc133valid.htm.